Development of a Hardware for Frequency Scanning Interferometry for Long Range Measurement

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***Abstract*— The advancement in optical technology based metrology has been significant over recent years. Many applications utilize the Frequency Scanning Interferometry (FSI) technique for short and long-range precision measurements. This paper discusses the design and development of a cost-effective FPGA based data acquisition solution for FSI system for long-range measurement. The proposed hardware uses the 160MS/s ADC interfaced with an FPGA via an LVDS interface. The acquisition hardware utilizes the external clock signal generated from the reference interferometer which reduces the non-linear effect of the tunable laser for improved precision. The design and development of a low noise comparator design for an external sampling clock is also presented.**

Keywords—FSI, Absolute long-range measurement, FPGA, Tunable Laser, High-Speed data acquisition, FIFO, Frequency Scanning Interferometry, LIDAR

I. INTRODUCTION

FSI is one of the common absolute distance measurement technique used for short-range precision measurement in commercial and industrial applications. The revolutionizing technique is used in medical imaging applications which is often adopted to sweep-source optical coherence tomography (SS-OCT) [2][3]. In recent years, the method has been extended for long-range measurement to measure absolute and simultaneous distance measurement. It is widely used in science and industrial projects, such as ATLAS particle detection at CERN Geneva [4][5], space missions requiring independent satellites working cooperatively[6], in aerospace industries where construction of aeroplanes and large objects, as well as the calibration machines and tools[7][8] to name only a few.

The simultaneous accurate distance measurement of multiple objects is one of the key benefits of utilising FSI. The optical frequency modulation technique using laser offers the possibility to measure the absolute distance of the order from several meters, to down to 10 μm[9], with a potential accuracy of less than 1 μm [10] with advancement in the measurement electronics. This advancement led to the possibility of measuring the moving targets/objects with some limitations [9][10]. The optical tunable laser source is one of the main signal sources used by FSI system for measurement. The constant rate of change in optical wavelength during the sweep period is preferred, and any fluctuation in scan rate during the measurement significantly impacts the measurement, such as in the case of the non-linear effect of the tunable laser source. The non-linear behaviour of the tunable laser source could be compensated during the measurement, which would improve the measurement accuracy. One of the techniques used is to generate the external trigger signal generated from the same laser source used as the sampling trigger signal [11]. However, there are a number of other methods proposed to overcome these challenges which were discussed in the literature [12][13][14].

A suitable FSI measurement hardware solution is required to measure extremely high-frequency signals when the interferometers are long and tuning rates of the measured distance are high, i.e in the range of several tens of MHz to hundreds of MHz. for those requirements the data acquisition and signal processing hardware are pushed to their performance boundaries to achieve the real-time measurement needs. Furthermore, most commercially available hardware that has matured for telecommunication and related industries[22], not for FSI measurement applications.

II. BASICS OF FSI BASED MEASUREMENT APPROACH

The FSI is effectively a LIDAR that uses the interferometer to measure the modulated optical frequency. There are number of FSI techniques that are used for absolute distance measurement for single target measurement. Nonetheless, the simultaneous measurement of objects using FSI systems have also been studied and demonstrated[15-18]. The resolution of μm grade measurement has benefited from the FSI approach. For the long-range measurement such as at 24 metres [8] and 20 metres ranges [19] with a measurement resolution of 65.5 μm and 40 nm sub-scan resolution using the calibrated longer gas cell are achieved respectively.

A. *The physical optical arrangement of an interferometry*

The FSI system uses the interferometer(s) to measure modulated light. The basic arrangements for a Michelson interferometer is illustrated in fig 1 below.

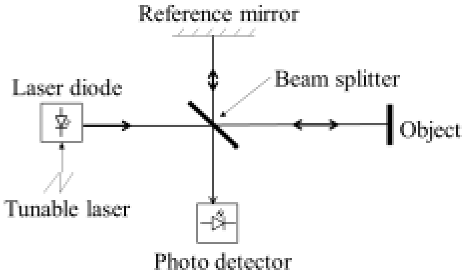

Fig. 2. Basic Michelson interferometry optical arrangement

The tunable laser light is emitted from the laser diode, usually after the collimated lens is split into two main beams by the beam splitter. One beam is focussed on the reference mirror, whereas the other is focussed on the object/target both reflected beams are coherently superimposed onto the photodetector. During the measurement, the tunable light source sweeps the optical frequency over a period of time. The absolute distance to the object creates the Optical Path Difference (OPD) which results in creating the phase difference between the incident wave and the reflected wave in order to generate the fringe pattern. Since the laser source sweeps the frequency over a fixed period of time (during the laser scan) the fringe pattern light intensity oscillates with respect to time. The frequency of the oscillation is proportional to the OPD and the tuning rate of the laser.

The current generated by the photodiode at an instant of time t can be expressed by equation 1 [15].

$$I(t,\tau) = A.\cos\,[2\pi(\alpha\tau t + f_0\tau)] \qquad (1)$$

Where α is the tuning rate of the laser, τ is the time of flight (time taken for the laser beam reflected back from the object), $\mathrm{f_0}$ is the optical frequency of the laser when $\mathrm{t} = 0$ and A is the amplitude of the detected signal which depends on the effective reflection coefficient. Understandably, the term $\alpha\tau$ contains the information about the oscillating photocurrent generated by the photodiode, when the target is assumed to be at a fixed distance or free from any vibrations. The relationship between the frequency of the signal generated by the photodiode $\mathrm{f_{beat}}$ and the distance to the target D is given by equation 2. Here it shows that the $\mathrm{f_{beat}}$ is directly proportional to the distance and inversely proportional to the tuning rate of the laser. Here c is the speed of light in the vacuum and ν is the optical frequency of the laser.

$$D = c\frac{f_{beat}}{2\alpha} \qquad (2)$$

$$\alpha = \frac{d\nu}{dt} \qquad (3)$$

When the target is in motion the term $\mathrm{f_0}\tau$ from the equation (1) becomes time-dependent [1][9]. The OPD of more than 40 meters of absolute distance with a higher tuning rate of 2000 nm/s for 30 nm bandwidth would generate more than 31 MHz f_{beat} frequency.

B. *The FSI measurement principle in respect to reference and reflected laser beam.*

The OPD between the reference and the reflected laser from the target/object creates the modulated frequency which can be used to detect the distance of the object. Fig 2 illustrates the basic measurement principles of the FSI technique. The reference laser beam (in blue) sweeps the frequency between $\mathrm{f_0}$ and $\mathrm{f_m}$ over the period t_1 at a rate α Hz/s. The reflected light from the target (in red) creates a modulated intermediate frequency ($\mathrm{f_{beat}}$) when the time delay τ due to light return time between source and target. Consequently $\mathrm{f_{beat}}$ will be dependant on the laser sweep rate(α). Furthermore, from equation (2) the intermediate frequency is proportional to twice the absolute target distance when the tuning rate of the laser is constant over the sweep period.

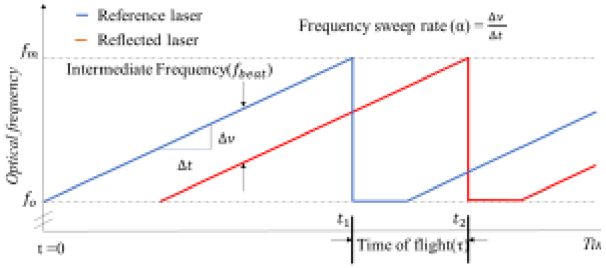

Fig. 1. The optical frequency of a reference and reflected laser as a function of time.

III. DESIGN AND DEVELOPMENT OF A DATA ACQUISITION HARDWARE FOR FSI

The data acquisition hardware used to measure the high-frequency signal generated by the FSI often requires high-performance computation hardware such as FPGA to meet the real-time needs of computation heavy data processing. The DSP techniques such as FFT are used to compute the frequency spectrum. The detection of peaks in the spectrum domain then enables the computation of the distance to the target. Hardware such as GPU with four to eight-lane PCIe bus systems has been identified as a potential solution to such systems [22] for GT/s data transfer rate between ADC and runtime systems for further processing. Such commercially available hardware platforms are often either expensive (several thousands of GBP) or require significant modifications for FSI applications.

A. *The high-speed ADC clock driver*

The non-linearity of the tunable sweep source has a direct impact on the measurement accuracy because the intermediate frequency varies over the measurement period, which directly affects the measurement of absolute distance. Several hardware and software techniques have been proposed to remedy this [14][20][21].

A major bottleneck in achieving high precision measurement is often the electronics systems used to measure the electrical signal generated by the optical sensors. One possible way to eliminate the non-linear effect of the tunable laser is to control the sampling rate and synchronise it with the tunable source. This is to generate an external sampling clock (also known as k-clock) from the same tunable source used by the FSI. Fig 3 illustrates the non-linear behaviour of a tunable source during a single sweep. This shows in red that the tuning rate over the sweep period is not constant but oscillates.

The non-linear effect is improved using second interferometry generating a trigger signal for the ADC [9]. This is often called a trigger or a reference interferometer. However, during the length of the scan period interferometer(s) and reference interferometer must be kept constant[16].

The photodetector detects the modulated signal from the reference interferometer and generates an oscillating sine wave. This trigger signal could be used as an external sampling clock for the measurement ADC. However, this is relatively a weak signal (usually several hundreds of mv peak-to-peak) and cannot be directly used as a clock. The comparator or sinewave to logic converter should be used to convert the signal into a CMOS logic signal interface.

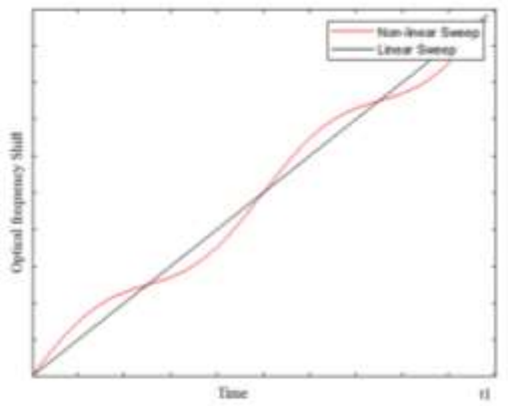

Fig. 3. Illustration of linear and non-linear optical frequency sweep source behaviour for the time period t1.

Tunable laser modules such as TLM-8700 provides feedback about the current tuning operation via a logic output signal “Sync”. Fig 4 shows how such an optical frequency tuning source provides the “Sync” signal to identify two sweeps. The delay δt exists when the laser source prepares for the second sweep such as preparing the mirror for the next scan. Active low sync signal from fig 4 indicates the valid tuning. It is essential to monitor this signal to identify the individual sweeps.

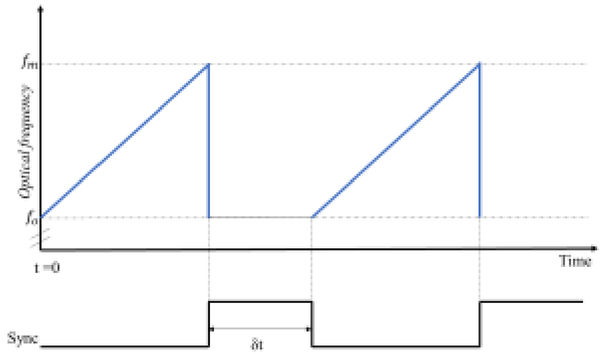

Fig. 4. Generated “sync” signal against the optical frequency sweep operation.

The data acquisition hardware must, therefore, be implemented in such a manner as to ensure that the acquired data is only valid during the scan.

1) *The Comparator*

The LTC6957-4 is a low phase noise buffer optimized to convert sinewave signals to CMOS logic levels. The lower phase noise of 140 dBcHz^{-1} at 100 Hz offset frequency device is particularly important as FSI systems are sensitive to electrical phase noise, especially when generated clock signal from the trigger interferometry containing phase noise which degrades the measurement, where the ADC is driven by the external sampling clock to correct the non-linearity of the laser. The 300 MHz input bandwidth device is designed for interfacing with differential input sine waves from the trigger interferometry. The small-amplitude input signal generates the CMOS logic signal that directly interfaced with the ADC clock input. The single supply device includes input filtering with three narrowband settings to limit the bandwidth of the input signal. Moreover, the generated clock signal from the comparator is synchronized with “Sync” signal from the tunable laser module to avoid any unwanted glitches to the ADC. Fig 5 explains such signal attributes.

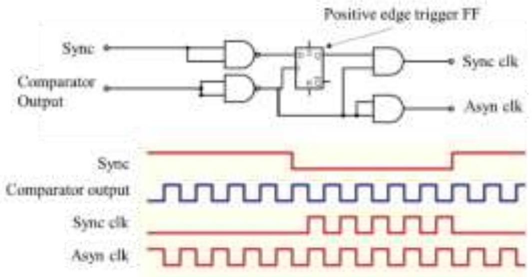

Fig. 5. Comparator output is synchronized with "Sync" signal from the tunable laser module using D-Type Flip-Flop

The positive edge-triggered flip-flop (FF) has been used to synchronize the sync signal and the output from the comparator (clock) which generates the external clock signal for the ADC. The comparator output and “Sync” signal is interfaced with the clock and the Data input of the FF respectively to synchronise the clock output. The two NAND and AND gates are used to match the propagation delay for the input and output signal.

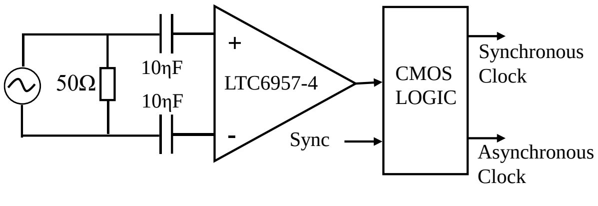

Fig 6: Simplified circuit diagram of the ADC clock driver

Fig 6 shows the simplified circuit diagram of the clock driver circuit. The LTC6957-4 comparator is interfaced with the output of the balanced photodetector (BPD) from the trigger interferometer. The comparator’s CMOS output is then controlled by the logic circuits shown in fig 5. Further, fig 7 shows the custom-developed PCB containing the LTC6957-4 and the relevant logic circuits onboard.

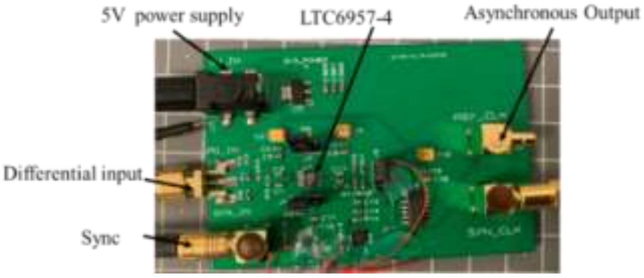

Fig.7. The custom-designed PCB for the ADC clock driver

This circuit was tested with National Instrument’s NI5752 digitizer adapter module (ADC) with FlexRIO. The NI-5752 clock was configured to an external clock and the clock signal from the circuit was used to measure a known signal generated from the NI PXI-5412 signal generator. Furthermore, the clock signal was analyzed using the frequency spectrum analyzer for clock jitter and phase noise.

B. The ADC module

The AD16DV160 digitizer was selected for this development. It is a 16-bit dual-channel monolithic 160 MS/s CMOS Analog to Digital converter. The programable device has LVDS outputs with Dual Data Rate (DDR). The differential external sampling clock provides optimum dynamic performance over a wide range of input frequencies. Fig 8 illustrates the functional block diagram of the proposed front end Data Acquisition System (DAQ) hardware with the ADC module interface.

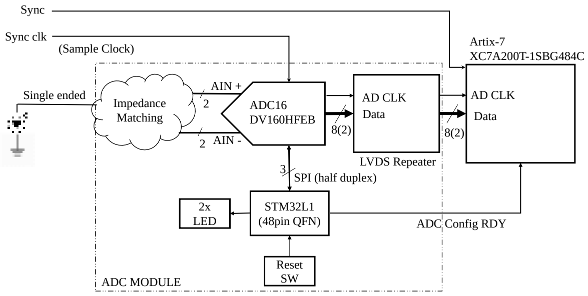

Fig. 8. Functional block diagram of the ADC module interfaced with Artix-7 FPGA via LVDS interface.

The single-ended signal from the photodiode to measure the interferometric output signal is interfaced with the ADC via the impedance matching circuit. The synchronous ADC clock (sync clk) signal is generated by the ADC clock driver to determine the number of samples obtained during the measurement. The 8-bit parallel data bus and the output sampling clock from the ADC is interfaced to the Xilinx Atrix-7 FPGA differential IOs via the Low Voltage Differential Signal (LVDS) repeater. The DDR sampling enables the 8-bit parallel data to be sampled for odd and even bits at the rising and falling edge of the clock respectively. The sync signal from the tunable laser module provides a valid data sweep information to the FPGA. The microcontroller (STM32L) is interfaced with the AD16DV160 via a 3-wire SPI interface that allows access to the control registers. This enables to configure clock phase adjustment, a fixed pattern generator and clock division for the ADC. During the initial start-up, the “ADC Config RDY” signal is asserted by the MCU to FPGA which in turn validates the ADC configuration before the acquisition process begins.

IV. RESULTS AND DISCUSSION

A. The clock generation circuit

The clock generation circuit was interfaced with the FSI systems and the National Instrument’s NI5752 digitizer module. The FSI acquisition setup has been explained in fig 9.

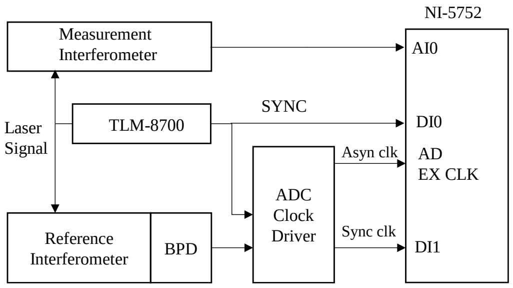

Fig. 9. The external clock and the Sync signal interfaced with NI-5752

The signal generated from the tunable laser module TLM-8700 is interfaced with the reference interferometer. The optical signal detected by the BPD generates sinusoidal signal. This is then processed through the ADC clock driver to generate the sampling clock for the digitizer (NI-5752). The asynchronous clock signal is used to drive the ADC while synchronous clock signals are used to count the number of sampling points over the valid laser sweep period via Digital input 1(DI1). The “Sync” signal from the TLM-8700 is also interfaced with DI0 to synchronize the data acquisition.

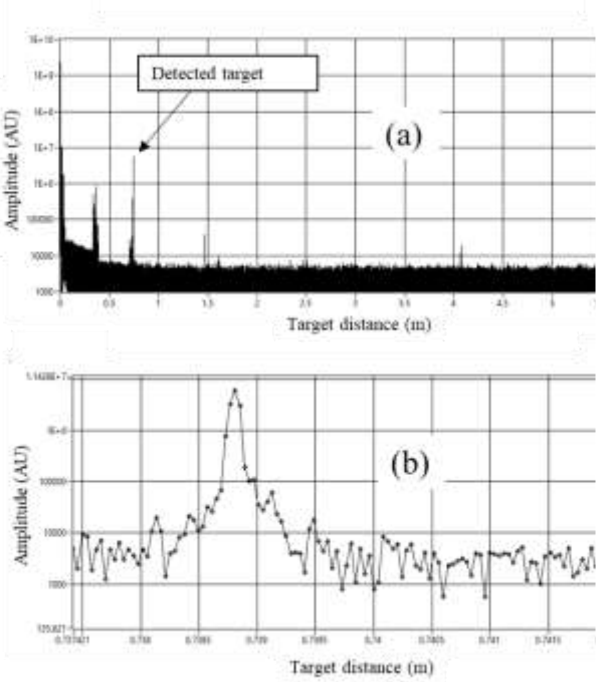

Fig.10. (a)Measured and computed FSI data using external clock signal provided by the reference interferometer, (b) magnified peak from (a)

Fig 10 shows the measured FSI data from the photodetector (measurement arm) at the object distance of 0.738808 m. Fig 10(a) and fig 10(b) shows the signal obtained between the range 0m to 5.606911 m, and the same signal between 0.737421 m to 0.742376 m respectively. During the measurement, the tunable laser module was set to tune between 1530nm and 1560nm at a tuning rate of 2000 nm/s. The measured OPD to the reference interferometer was 22.44 m, the distance was achieved via single-mode fibre (SMF), which in return produces the sampling clock. The direct measurement range between 0 and 5.606911 m with a resolution of 40 µm was achieved from this experiment.

B. FPGA based simple high-speed DAQ verification

The proposed ADC module in fig.8 requires the data acquisition hardware to measure the high-speed digitized signal. FPGA based simple Data Acquisition (DAQ) systems have been developed to buffer the data before the samples are sent out for further processing on PC. The simplified block diagram of a developed digital hardware system is shown in fig11.

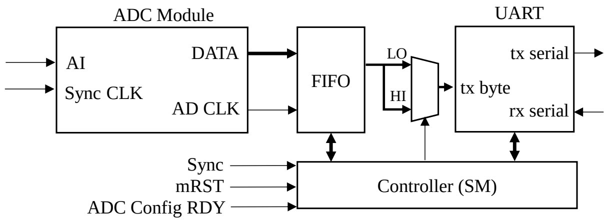

Fig. 11. Block diagram of the designed hardware for simple high speed DAQ system.

The ADC module is interfaced with the independent clock Block RAM(BRAM) based 131,072 size FIFO with 16-bit data width. The 16-bit DDR ADC data is acquired using the AD CLK via the 8-bit LVDS interface. The multiplexer multiplexes the 16-bit FIFO data into two bytes (HI and LO) before transmitting the bytes through the simple full-duplex UART at a baud rate of 115200. The state-machine based controller generates the control signal throughout the acquisition process.

Fig. 12. The Sync(AD_Sync), ADC Config RDY(ad_config_rdy) in respect to FIFO read/write operation as well as data transmitted via UART serial transmission(TX_SERIAL)

Figure. 12 shows the simulation results for the developed hardware, further, part of the simulation also shows the asynchronous signals “Sync”, and “AD config rdy” signals are used to acquire the 16-bit simulated data from the ADC module where, the data is written into and read out from the FIFO. The “r_wr_data_count” signal shows the number of data being written into the FIFO during a write operation in respect to the “Sync” signal at the same time the “fifo_wr_en” signal is de-asserted after 3 clock cycles in respect to sync signal transition. The simulation also confirms that the UART serial transmission is synchronized with the FIFO read operation. The simulation also shows that the 16-bit data from the FIFO is split into HI (MSB first) and LO (LSB last) before 8-bit serial data is transmitted.

V. CONCLUSION

This paper discussed the development of an FPGA based simple real-time hardware acquisition system for the FSI based measurement of the absolute distance of a target at a distance of more than 5 meters. In particular, we have examined the data acquisition process and the use of a trigger interferometer to improve the non-linear effect of the tunable laser source used in this application. The development of an ADC clock driver which uses the reference interferometric signal from the BPD to generate a clock signal which is suitable for the ADC external clock was demonstrated. The design and development of a high-speed FIFO based data acquisition system that acquires and transmit the ADC data via a simple UART was also demonstrated. The proposed system has the potential to be extended to measure target distances of more than 35 meters, using the PCIe interface (Replacing the UART) which will be the focus of future work.

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